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JOURNAL OF APPLIED PHYSICS **118**, 045307 (2015)

Comparison of gate dielectric plasma damage from plasma-enhanced atomic layer deposited and magnetron sputtered TiN metal gates

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Fully depleted silicon-on-insulator transistors were fabricated using two different metal gate deposition mechanisms to compare plasma damage effects on gate oxide quality. Devices fabricated with both plasma-enhanced atomic-layer-deposited (PE-ALD) TiN gates and magnetron plasma sputtered TiN gates showed very good electrostatics and short-channel characteristics. However, the gate oxide quality was markedly better for PE-ALD TiN. A significant reduction in interface state density was inferred from capacitance-voltage measurements as well as a 1200× reduction in gate leakage current. A high-power magnetron plasma source produces a much higher energetic ion and vacuum ultra-violet (VUV) photon flux to the wafer compared to a low-power inductively coupled PE-ALD source. The ion and VUV photons produce defect states in the bulk of the gate oxide as well as at the oxide-silicon interface, causing higher leakage and potential reliability degradation. © *2015 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4927517]

I. INTRODUCTION

Metal gate materials have now replaced polysilicon gates for advanced silicon CMOS fabrication of both planar silicon MOSFETs and FinFETs. However, plasma processes employed for metal gate deposition can cause significantly more damage to the gate dielectric material than with traditional chemical vapor deposition (CVD) polysilicon gates, resulting in reduced device performance and reliability. Titanium nitride (TiN) is used for metal gates because of its thermal stability and compatibility with gate dielectric materials. Additionally, the workfunction of TiN can be tuned across a wide range enabling high-workfunction TiN for low threshold voltage (V_t), high performance pMOSFETs,[1,2] low-workfunction alloys of TiN for low V_t, high performance nMOSFETs, or mid-gap TiN metal gates for undoped-body fully depleted silicon-on-insulator (FDSOI) transistors for subthreshold, ultra-low power operation.[3,4]

TiN is frequently deposited by plasma sputtering though atomic layer deposition (ALD) is now sometimes employed, particularly in replacement gate processing. Processes for depositing TiN thin films by thermal ALD[5–13] or plasma-enhanced ALD (PE-ALD)[8,10,14–25] have been presented in other work, summarized in two excellent ALD review articles by Profijt[26] and by Miikkulainen.[27] The current paper compares gate dielectric quality, including interface trap formation and gate leakage, of devices fabricated with traditional plasma sputtered TiN and PE-ALD TiN. The organization of the paper is as follows. First, physical characteristics of the two films such as resistivity, composition, and morphology are compared. Second, the gate dielectric quality is examined by measurements on MOS capacitors. Finally, electrostatic performance of long- and short-channel FDSOI transistors are presented.

II. EXPERIMENTAL

An Oxford Instruments OpAL system was used for PE-ALD using tetrakis(dimethylamido)titanium (TDMAT) and an H_2/N_2 plasma mixture as precursors. The plasma and N_2 purge times were 10 s and 2 s, respectively. TDMAT was heated to 50 °C and bubbled with 200 sccm Ar. The plasma was generated by applying 300 W of 13.56 MHz RF power to an inductive coil surrounding a sapphire tube. The plasma gas flow rates were 40 sccm N_2 and 10 sccm H_2. Plasma magnetron sputtered TiN films were deposited at 300 °C using an Electrotech Sigma system, operating with 6 kW RF power, in pure N_2 gas using a Ti target. Blanket films were deposited on 100 nm thermally grown SiO_2 on 200 mm silicon wafers.

Accurate thickness measurement of the thin TiN film requires careful consideration. A Kramers-Kronig consistent optical model for the TiN was extracted from measurements made by a Wollam spectroscopic ellipsometer. The model was input to a KLA UV1280 ellipsometer, which was used to measure 49 points across each sample. The ellipsometric thickness measurements showed excellent correlation with transmission electron microscopy (TEM) measurements performed on several samples. Based on the TEM measurements, a small thickness offset correction was applied to the ellipsometer data. The TEM-corrected ellipsometer measurements were compared to measurements performed using an Oxford X-Strata 980 x-ray fluorescence (XRF) system, which measures the total Ti content of the film. The correlation between the two measurements was excellent, suggesting that the film thickness measurements are accurate. TiN sheet resistance measurements were performed using a 4-point probe, and the

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resistivity was calculated using the thickness measured by ellipsometry.

1 mm^2 capacitors were fabricated on 200 mm p-type silicon wafers with 3.5 nm thermally grown SiO_2 as the gate oxide. The capacitor top electrode is formed from 20 nm TiN capped with 120 nm of phosphorous-doped polysilicon. Ultra-low power FDSOI transistors were fabricated as described in detail elsewhere.[1,2] The transistor gate stack is the same as on the capacitors. Transistors of multiple dimensions were fabricated and measured, but results reported in this work are limited to devices with W = 2 μm and L = 90–300 nm.

III. RESULTS AND DISCUSSION

A. TiN film comparison

The sputtered TiN film properties show little variation across various process parameters. TOF-SIMS analysis shows a film composition of 49% N and 51% Ti, with oxygen concentration in the bulk of the film below detection limits. Sputtered TiN resistivity is 0.13 mΩ cm. The films are largely amorphous, with an evidence of some weakly columnar grain structure. Grain sizes are on the order of 5–10 nm (see Fig. 3).

Characterization of the PE-ALD films is more involved, as the material properties are expected to be sensitive functions of deposition process variables. To match the sputtered film properties as closely as possible, the effects of TDMAT dose time and deposition temperature were investigated. Figs. 1(a) and 1(b) show the effect of varying the TDMAT dose and the number of cycles, respectively, on the TiN thickness. At lower temperatures, the TiN thickness increases modestly with increasing TDMAT dose time, but at higher temperature the thickness increases rapidly with TDMAT dose. Non-saturating behavior indicates that some CVD-like growth is occurring in parallel with the ALD reaction mechanism, as is common for organometallic precursors such as TDMAT.[8,27] CVD-like growth occurs when the precursor thermally decomposes on the wafer surface rather than chemisorbing to the surface or, more properly stated, when the precursor decomposes on a faster timescale than an ALD deposition cycle. The rate constant of TDMAT decomposition[28] increases rapidly above 270 °C,[28] consistent with the growth curves in Fig. 1(a) where the 200 °C and 250 °C cases nearly saturate but the 300 °C case does not. Fig. 1(b) confirms that TiN thickness increases linearly with the number of cycles at 200 °C and 250 °C, indicative of ALD-like growth,[27] but at 300 °C, the growth-per-cycle increases with the number of cycles indicating a significant CVD-like growth component.

Fig. 1(c) shows that resistivity is independent of dose time for times as short as 0.5 s, indicating that the film stoichiometry is largely independent of dose as should be true of an ALD process. In Fig. 1(d), the film resistivity decreases as the thickness increases, reaching a nearly constant value for thickness above 20 nm. The resistivity is significantly higher for films deposited at 200 °C and for very thin films.

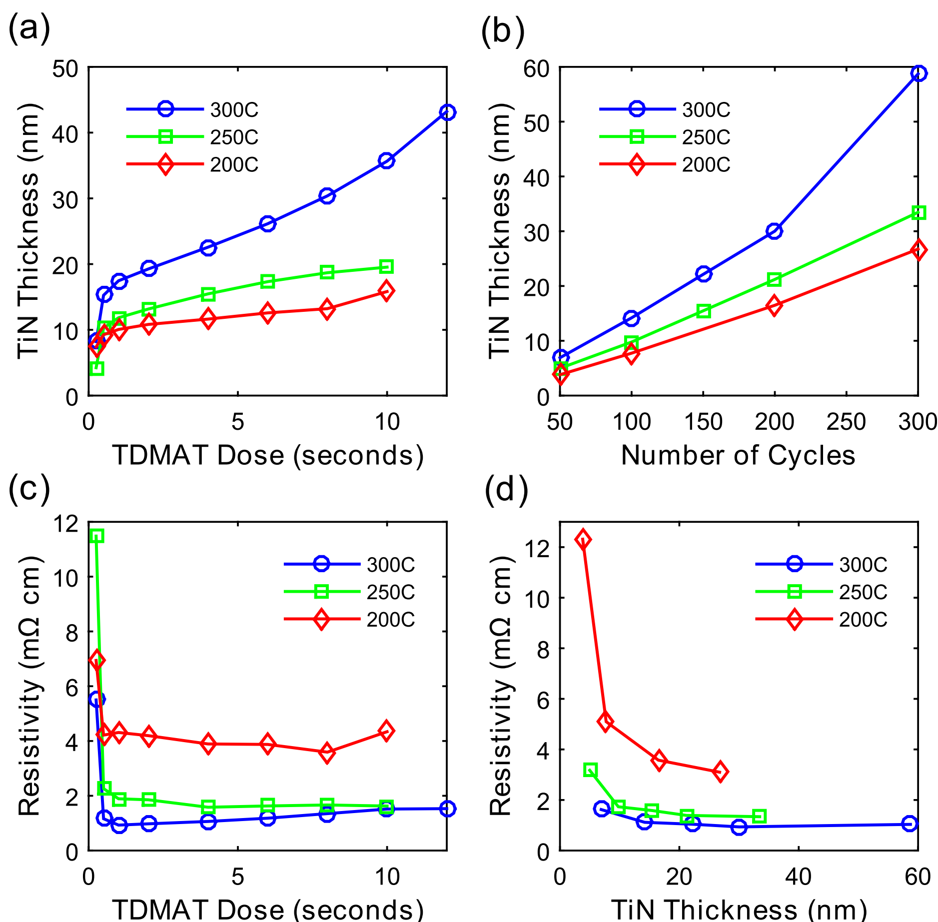

FIG. 1. Characterization of the TiN PE-ALD process. (a) TiN thickness as a function of TDMAT dose after 150 cycles. (b) TiN thickness vs number of cycles for 4 s TDMAT dose. (c) Resistivity of the same films deposited in (a). (d) Resistivity of the same films deposited in (b).

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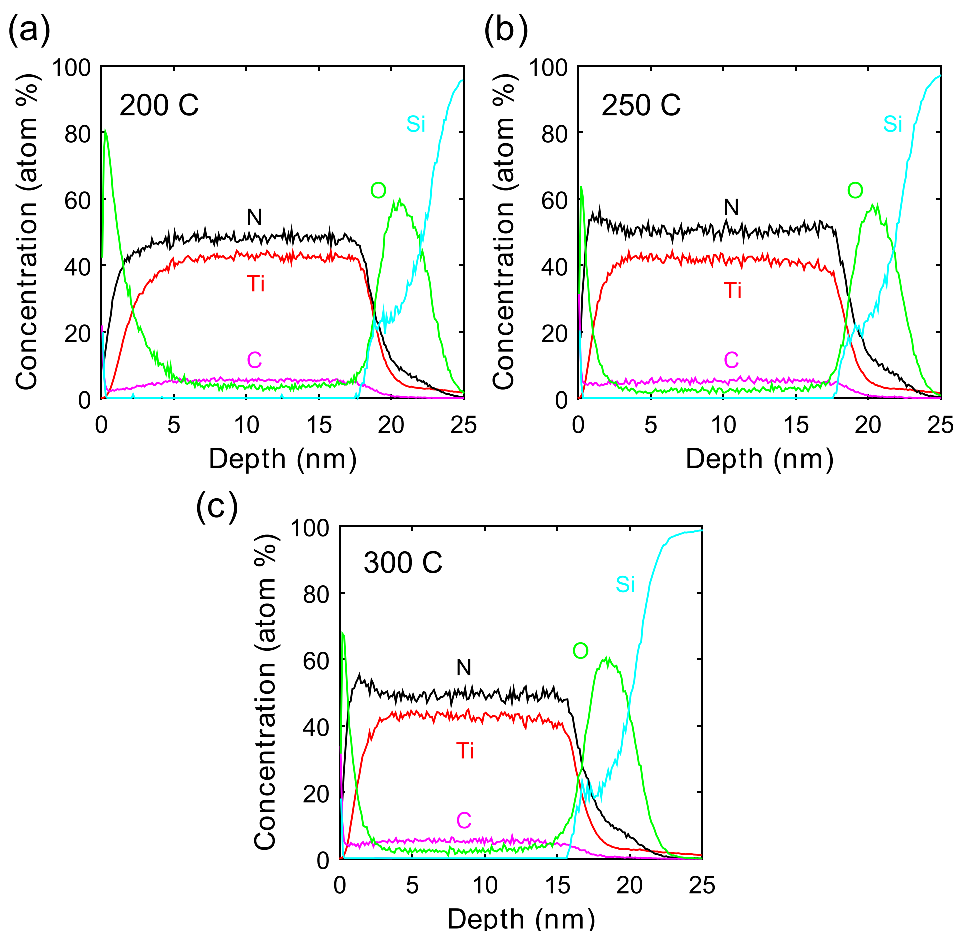

FIG. 2. SIMS analysis of PE-ALD TiN films deposited at (a) 200 °C, (b) 250 °C, and (c) 300 °C.

TOF-SIMS analysis for PE-ALD TiN deposited at three different temperatures are shown in Fig. 2, and the atomic composition in the bulk of the film (several nm from either interface) is provided in Table I. The Ti, N, and C composition of films deposited at 200, 250, and 300 °C are quite similar. The high resistivity of the 200 °C film (Fig. 1(c)) is attributed to higher oxygen content. An increase in O atom concentration from 2.5% to 3.5% causes more than 2-fold increase in TiN resistivity. The bulk film oxygen content arises due to competing surface reactions between O and N during TiN film growth. As the temperature decreases, the Ti + N reaction rate decreases faster than the Ti + O reaction rate, resulting in a more oxygen incorporation. Though oxygen is not intentionally introduced into the process, it is present in low concentration from residual water on chamber surfaces and from plasma bombardment of the sapphire plasma tube.

It is also seen in Fig. 2 that the surface of all three films is highly oxidized. The thickness of this oxidized layer is greatest for the lowest temperature film. This explains the high resistance values of the very thin films in Fig. 1(d), as these films are substantially TiON. Surface oxidation occurs after film exposure to the environment and occurs at a faster rate in low temperature films due to their lower density.[5,9,11]

TABLE I. Elemental composition of TiN films deposited at different temperatures, in atomic %.

	Ti	N	C	O
200 °C	42.6	48.3	5.5	3.5
250 °C	41.7	50.3	5.3	2.5
300 °C	42.9	49.1	5.4	2.4

The resistivity data were fit to a bilayer stack model of a thin high resistivity TiON film on top of a low resistivity TiN film. The best-fit thickness of TiON is 4.1, 3.2, and 2.7 nm and the best-fit bulk TiN resistivity is 2.6, 1.2, and 0.8 mΩ cm for the 200, 250, and 300 °C films, respectively.

Fig. 3 shows TEMs for a deposition condition of a 4 s TDMAT dose with 150 cycles at several temperatures. The morphology of the PE-ALD TiN film is similar to that of the sputtered TiN film.

It was not possible to match the composition and resistivity of the sputtered and PE-ALD TiN films exactly, since no PE-ALD conditions could eliminate the carbon and oxygen content completely. PE-ALD deposition conditions of 4 s TDMAT dose at 300 °C provided the highest Ti content, lowest O content, and lowest resistivity, thus these conditions were used for fabrication of electrical devices.

B. MOSCAP comparison

MOS capacitors were fabricated to examine the interface quality and to compare gate dielectric damage between PE-ALD and plasma sputtered TiN. Figs. 4(a) and 4(b) show representative high-frequency CV measurements of MOSCAPs fabricated with sputtered and PE-ALD TiN, respectively. The points represent measurements and the

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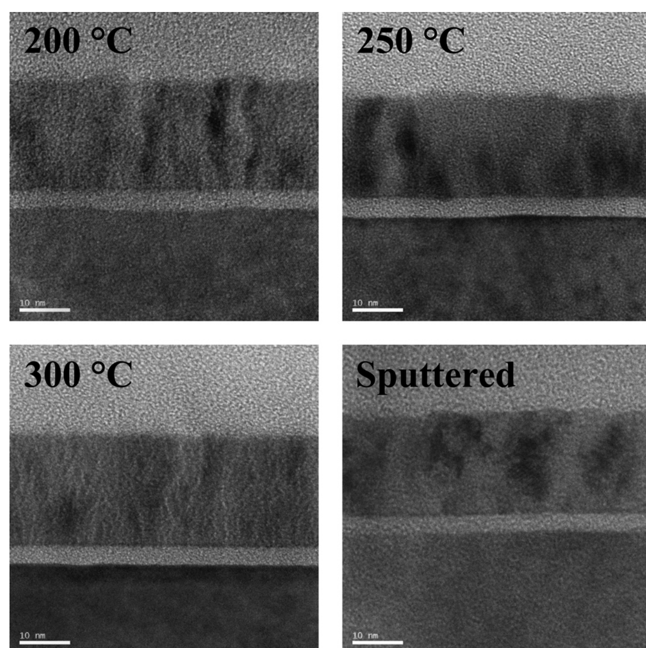

FIG. 3. TEMs of the PE-ALD TiN film deposited at 200, 250, and 300 °C, as well as a plasma sputtered TiN film.

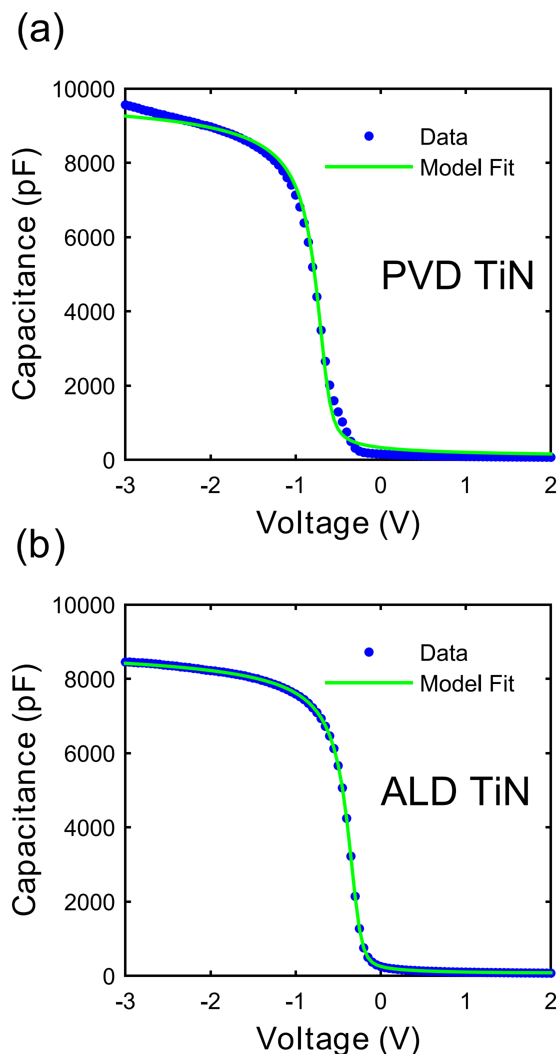

FIG. 4. The capacitance-voltage characteristics of $1 \times 1\,\text{mm}^2$ capacitors deposited with PVD TiN (a) and ALD TiN (b) showing the measured data points and a model fit.

solid lines are a best fit to a quantum-corrected model.[29] The PE-ALD TiN CV measurements are well fit by the model with a residual error of 0.6%, whereas the plasma magnetron sputtered TiN CV curve is distorted compared to the model resulting in a residual error of 4.1%. Stretching of the C-V curve as seen in Fig. 4(a) is characteristic of a high density of defect states (D_{it}).[30] The inductively coupled plasma configuration of the PE-ALD system results in a relatively low ion flux to the wafer surface, and the ions which do reach the surface are not energetic as they are largely thermalized by collisions in the space between the plasma region and the wafer. By contrast, in the sputtering system, a high power, low pressure magnetron plasma is a source of damaging energetic ion and vacuum ultra-violet (VUV) photons. These energetic species damage the underlying gate dielectric, giving rise to the increased D_{it} inferred from Fig. 4(a) compared to the results from the gentler PE-ALD process shown in Fig. 4(b).

A second indirect measure of charge traps in the gate dielectric is obtained from hysteresis in CV curve measurements. Hysteresis was measured by sweeping the gate voltage from 0 V to −3 V, to +2 V, and back to 0 V, then comparing the voltage at which the capacitance is equal to one-half the maximum value for the forward and reverse sweeps, as shown in Figure 5(b). Hysteresis arises from traps in the oxide or at the oxide/Si interface. In the present case, hysteresis in the CV curve evolves in the counter-clockwise direction as the gate voltage is swept from positive to negative and back to positive, consistent with electron injection from the silicon into defect states in the oxide.[31] Median hysteresis of sputtered TiN capacitors (−35 mV) is twice as large as that of PE-ALD TiN capacitors (−18 mV), indicating a higher density of slow traps in the gate dielectric of devices fabricated with sputtered TiN.

Figure 5(c) shows thicker equivalent oxide thickness (EOT) measured on PE-ALD TiN capacitors (3.71 nm) than on sputtered TiN capacitors (3.34 nm). The SiO_2 gate dielectric was grown on all four wafers simultaneously and subsequent processing was identical except for the method of TiN deposition, so the EOT difference must be a result of the TiN deposition process. The physical SiO_2 thickness after deposition was measured by TEM, as shown in Figure 6. For a 300 °C TiN deposition, there is no significant difference in physical SiO_2 thickness between sputtered and PE-ALD TiN films. Furthermore, the TEM-measured thickness of both films is the same as that measured when the TiN is replaced with a polysilicon gate. In all three of these cases, the mean physical film thickness is 3.50 ± 0.05 nm.

In the case of plasma sputtered TiN, the electrical gate oxide thickness is 0.16 nm smaller than the physical thickness, suggesting that Ti is implanted into the SiO_2 during the deposition process, increasing the effective dielectric constant (k) of the film. In the case of PE-ALD TiN, the electrical gate oxide thickness is 0.21 nm greater than the physical thickness. This is consistent with the presence of a thin,

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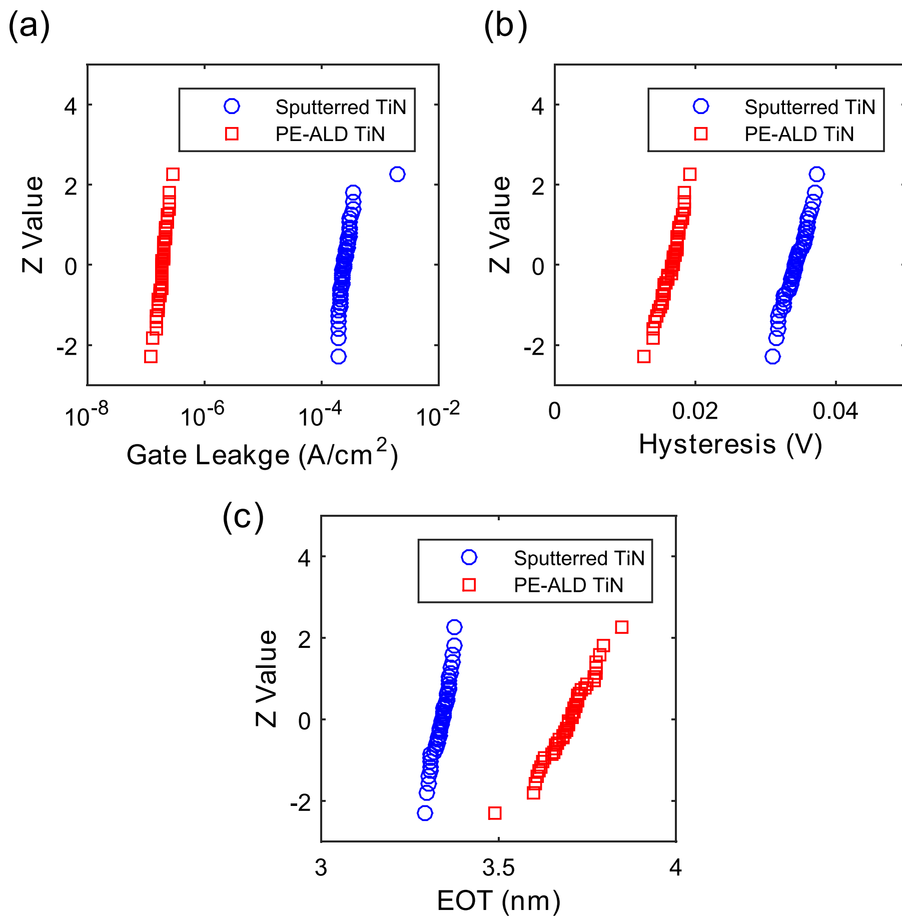

FIG. 5. Normal probability plots of electrical parameters extracted from sputtered TiN and PE-ALD TiN capacitors, (a) DC leakage current measured at 2 V below V_{fb}, (b) hysteresis between forward and reverse CV sweeps, (c) extracted equivalent oxide thickness.

insulating TiOCN layer formed at the beginning of the PE-ALD TiN growth process. Assuming an effective k of 15, the measured additional capacitance corresponds to a 0.85 nm thick TiON film. The SIMS data in Figure 3(c) confirm a mixed TiOCN layer at the TiN/SiO_2 interface. This layer is approximately 1 nm thick, in rough agreement with the above prediction from the electrical data, though it should be noted that it is not practical to quantify the thickness of this layer precisely from SIMS data due to the knock-on effect.

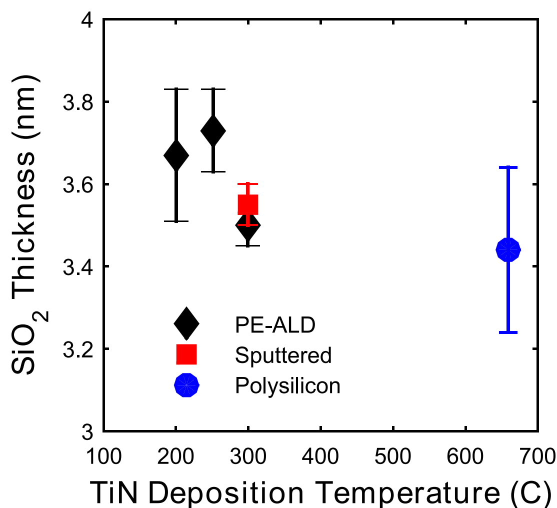

FIG. 6. Gate oxide thickness measured by TEM after TiN deposition by plasma-enhanced ALD and plasma sputtering. Gate oxide thickness after CVD polysilicon deposition shown for comparison.

The normal probability plot of capacitor leakage current in Figure 5(a) indicates that the PE-ALD capacitors exhibit 1200× lower median leakage current than sputtered TiN capacitors, both measured at 2 V below V_{fb}. Since the SiO_2 thickness as measured by TEM is the same for the PE-ALD TiN and sputtered TiN capacitors, the lower leakage is not due to a physically thicker gate oxide. Even if one considers the uncertainty in the SiO_2 thickness TEM measurements and takes the PE-ALD TiN case to be at the upper end of the thickness range and the sputtered TiN case to be at the lower end of the range, the SiO_2 physical thickness difference would be less than 0.4 nm. This would correspond to a maximum 30× difference in leakage current based on literature data.[32] Instead, the leakage current is primarily due to gate oxide damage which occurs upon exposure of the film to the magnetron sputtering environment. Ions and VUV photons have sufficient energy to break Si-O bonds in the SiO_2 gate dielectric, creating dangling bonds which permit significant leakage through the trap-assisted tunneling mechanism.[33] Additionally, Ti incorporation into the gate dielectric during the gate deposition processes would be detrimental to gate oxide quality and would result in increased gate leakage. Limitations in the SIMS data do not allow us to quantify the difference in Ti profile in the thin gate dielectrics, though some fraction of the increased leakage observed in the sputtered TiN capacitors is likely related to inadvertent Ti implantation.

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When using the measured leakage current as in indicator of gate oxide quality, care should be taken to ensure that appropriate gate voltages are employed. The data reported above are taken with V_g at 2 V below the median flat-band voltage for the two different types of capacitors to account for the effective work function difference between the two metals, as opposed to using the same absolute gate voltage for both types. A second-order correction can be introduced by considering that the thin TiON layer at the top of the PE-ALD gate and the thin TiOCN layer at the bottom of the PE-ALD gate may act as voltage dividers such that the electric field across the SiO_2 gate dielectric is lower in the PE-ALD TiN case. This would unfairly bias the PE-ALD capacitors toward lower gate leakage. Applying a somewhat worst-case set of assumptions where the top layer is 2.7 nm thick, the bottom layer is 1 nm thick, and k = 15 for both layers, to achieve the same field across the 3.5 nm SiO_2 gate oxide the gate voltage on the PE-ALD TiN capacitors should be 0.4 V higher (more negative). At this condition, the median measured leakage current is 715 nA/cm^2, which is significantly larger than the 200 nA/cm^2 reported in Figure 5; however, it is still far below the 240 μA/cm^2 measured on the sputtered TiN capacitors.

C. MOSFET comparison

Figs. 7(a) and 7(b) show drain current versus gate voltage curves for MOSFETs fabricated with sputtered and PE-ALD TiN, respectively. Each transistor has a gate width of 2 μm, gate length of 90 nm, and applied drain voltages of $V_{dd} = 0.05$ V and $V_{dd} = 0.3$ V. Both nMOS and pMOS transistors display well-behaved characteristics. Based on the threshold voltages, the effective workfunction of sputtered TiN is 4.71 eV and the effective workfunction of PE-ALD TiN is 4.56 eV. The difference is due to the carbon and oxygen content in the PE-ALD TiN film.[23] It may be possible to use the carbon and oxygen content to tune the TiN workfunction to achieve multiple threshold voltages, for example, if suitable process parameters can be identified.

Short channel performance is shown in Figs. 8(a)–8(c) which present the effect of gate length on subthreshold swing (S), drain-induced barrier lowering (DIBL), and threshold voltage roll-off, respectively. The short channel characteristics are nominally quite similar for the PE-ALD TiN and sputtered TiN transistors. For short gate length, S is slightly higher (by about 2 mV/decade) for the PE-ALD devices than for the sputtered devices. This increase can be explained by the slightly higher EOT of the PE-ALD transistors (see the Appendix).

For nMOS transistors, DIBL is nearly identical for sputtered and PE-ALD devices. For pMOS, it is about 40 mV/V higher for PE-ALD transistors at short L, again due to the higher EOT.[34,35] V_t roll-off is well controlled for both sputtered and PE-ALD TiN down to the smallest measured gate length of 90 nm. As noted above, the V_t shift between PE-ALD and sputtered transistors is due to a lower effective workfunction for PE-ALD TiN.

The transistor data show comparable median performance with both PE-ALD and sputtered TiN transistors, but

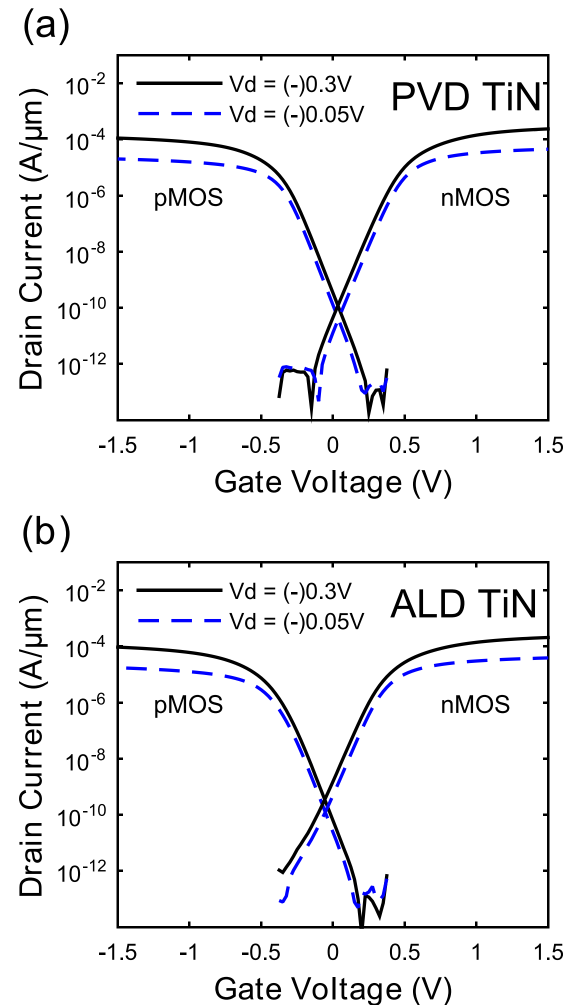

FIG. 7. The drain current versus gate voltage curves for sputtered TiN (a) and PE-ALD TiN (b) with the drain voltage for NMOSFETs (PMOSFETs) at (-) 0.3 V and (-) 0.05 V. L = 90 nm and W = 2 μm.

the distribution of gate leakage currents shows a significant difference. Normal probability plots of gate leakage measured at $V_g = 1.2$ V ($V_d = V_s = 0$ V) for both nMOS and pMOS transistors are shown in Figures 9(a) and 9(b). The distribution of gate leakage current is clearly tighter for the PE-ALD transistors. The data are separable into "good" transistors with less than 10^{-2} A/cm^2 gate current, and "bad" transistors with gate current 3 orders of magnitude higher. The sputtered TiN gates demonstrate a statistically significant higher probability of gate leakage, which is consistent with some form of gate oxide damage.

Transistors with a larger gate width (Figures 9(c) and 9(d)) still show a significant difference in gate oxide failure probability between sputtered TiN and PE-ALD TiN gates. However, the overall number of failed devices is lower than for smaller gate width devices. The wide devices (W = 2000 nm) have a 10 times lower antenna ratio than the narrow devices (W = 200 nm), since the area of metal pads and wiring is the same for all of these test transistors. This suggests that the gate oxide damage mechanism is sensitive to antenna ratio, which is characteristic of plasma induced damage.

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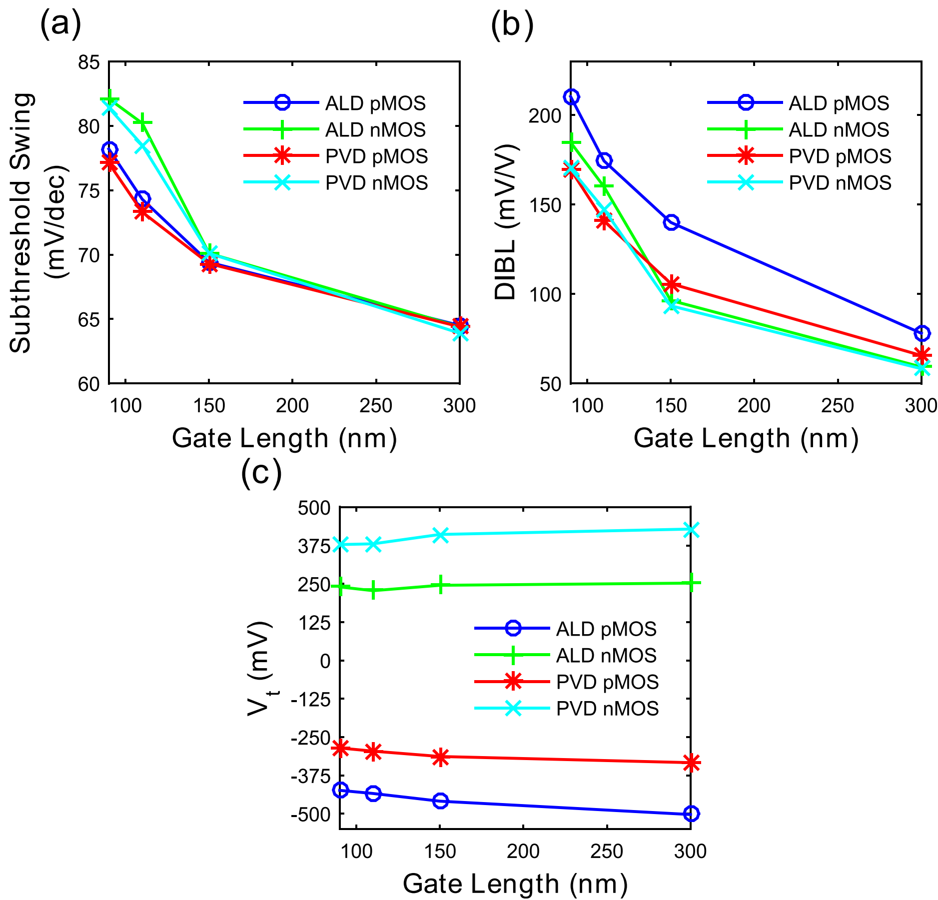

FIG. 8. The dependence of the subthreshold swing (a), drain induced barrier lowering (b), and threshold voltage (c) on the gate length for sputtered (PVD) and ALD TiN gates in nMOS and pMOS transistors.

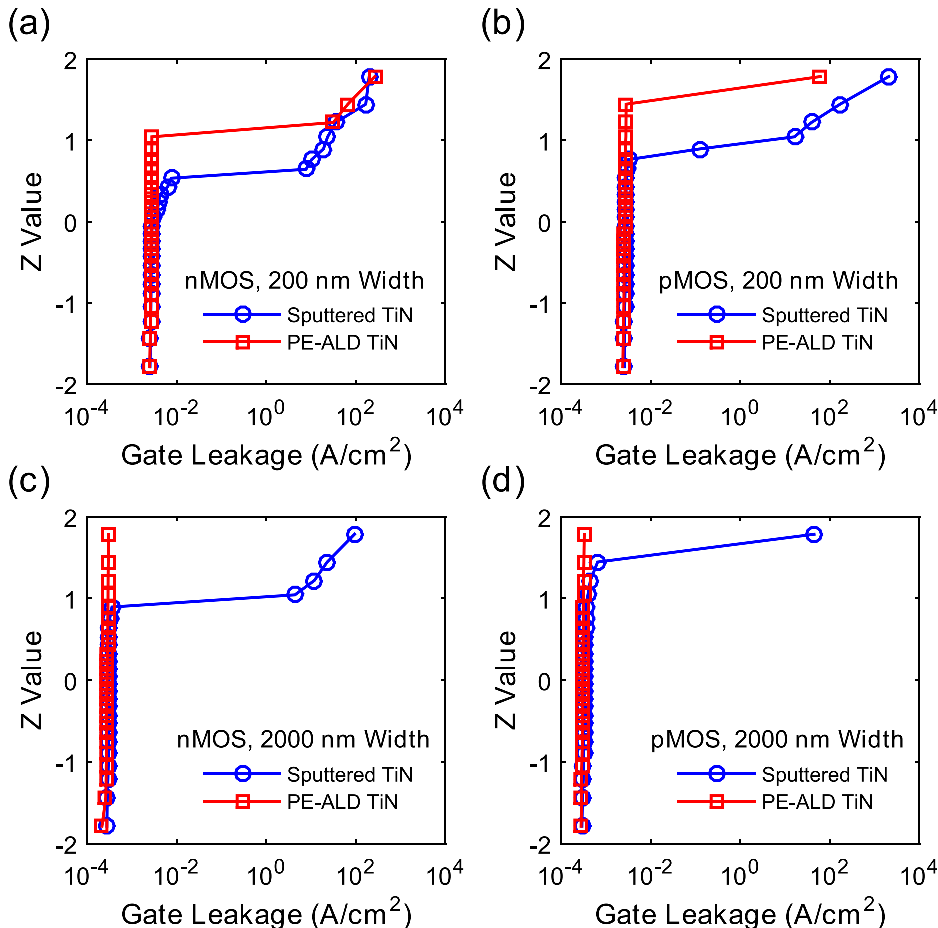

FIG. 9. Normal probability plots of gate leakage from nMOS and pMOS transistors, L = 120 nm, with a gate voltage of 1.2 V. (a) and (b) W = 200 nm-wide transistors, (c) and (d) W = 2000 nm-wide transistors.

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IV. SUMMARY AND CONCLUSION

Gate dielectric quality remains critical for advanced device fabrication, particularly for low power, low leakage devices. This work compared plasma-induced gate oxide damage by two different metal gate deposition processes: magnetron sputtering and PE-ALD. FDSOI transistors fabricated with either gate deposition process showed similar electrostatic performance, with very good short channel performance including subthreshold swing, DIBL, and V_t roll-off. However, gate dielectric quality metrics were significantly better when PE-ALD TiN was used compared to plasma sputtered TiN. CV measurements exhibited stretching of the curves and increased hysteresis with sputtered TiN compared to PE-ALD TiN, indicative of a higher density of interface states in the former case. In addition, gate leakage was 1200× higher for the plasma sputtered TiN devices, which is consistent with a high density of defects in the bulk SiO_2 leading to trap-assisted tunneling. Finally, transistors fabricated with both methods show that those fabricated with PE-ALD TiN demonstrate a significantly lower gate oxide failure probability. Taken together, the electrical results suggest that with plasma sputtered TiN the gate dielectric is damaged by energetic ions and VUV photons which break Si-O bands and leave defects states. In addition to higher leakage, these defect states can lead to device reliability issues and high early failure rates. By contrast, inductively coupled plasma PE-ALD produces a much lower energetic ion and VUV flux at the wafer surface, resulting in markedly less damage. Instead of damaging the gate oxide, PE-ALD initially deposits a sub-nm TiOCN film which may serve as a passivation. This layer does not seem to induce any undesirable device characteristics except for a very slight increase in EOT.

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APPENDIX: SUBTHRESHOLD SWING DEPENDENCE ON OXIDE THICKNESS AND GATE LENGTH

The subthreshold swing (S) of an ideal long-channel MOSFET is given by

$$S \equiv \frac{\partial V_g}{\partial(\log(I_d))} = \frac{kT}{q}\ln 10, \tag{A1}$$

where k is Boltzmann's constant, T is temperature, and q is the electronic charge. Several corrections can be applied to Eq. (A1) to account for effects of finite geometry and the presence of interface states.

Godoy *et al.*[36] derived a correction factor, $1/\lambda$, to account for barrier lowering due to short channel length

$$\lambda = 1 - \frac{[2(V_{bi} - \psi_{SL}) + V_{ds}]\tanh\frac{L}{2l}}{\sqrt{4(V_{bi} - \psi_{SL})(V_{bi} - \psi_{SL} - V_{ds})\sinh^2\frac{L}{2l} - V_{ds}^2}}, \tag{A2}$$

where V_{bi} is the built-in potential between the source-substrate and drain-substrate junction, ψ_{SL} is the surface potential of a long-channel MOSFET, V_{ds} is the drain-source voltage, L is the channel length and l is the characteristic length. For FDSOI MOSFETs, the characteristic length is given by

$$l = \sqrt{\frac{\epsilon_{si} t_{ox} t_{si}}{\epsilon_{ox}}}, \tag{A3}$$

where ε_{si} and ε_{ox} are the permittivity of silicon and the oxide, respectively, and t_{si} and t_{ox} are the SOI thickness and oxide thickness, respectively. When $V_{ds} \ll V_{bi} - \psi_{SL}$, λ can be approximated as

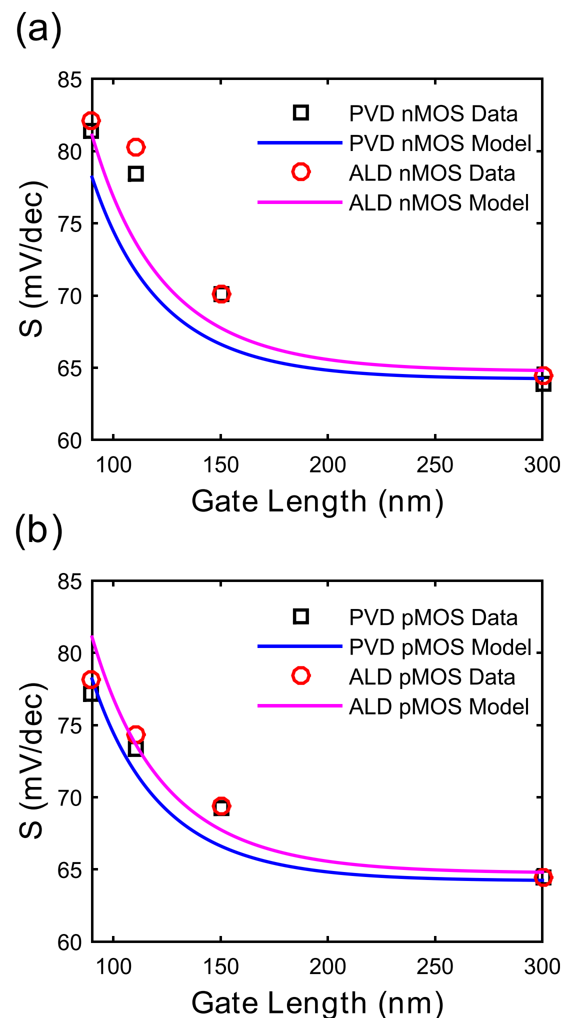

FIG. 10. Data (points) and model calculation (solid lines) for subthreshold swing of PE-ALD and sputtered (PVD) TiN NMOS (a) and PMOS (b) transistors.

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$$\lambda \cong 1 - \frac{1}{\cos h\left(\frac{L}{2l}\right)}. \tag{A4}$$

Balestra *et al.*[37] derived a correction factor to (A1) for FDSOI devices to account for finite BOX thickness and the presence of interface states

$$C^{-1} = \frac{C_{ox1}(C_{Si} + C_{ss2} + C_{ox2})}{C_{Si}(C_{ss1} + C_{ox1}) + (C_{ss2} + C_{ox2})(C_{ox1} + C_{ss1} + C_{Si})}, \tag{A5}$$

where $C_{ox1} = \varepsilon_{ox}/t_{ox}$, $C_{ox2} = \varepsilon_{ox}/t_{box}$, $C_{Si} = \varepsilon_{Si}/t_{Si}$, $C_{ss1} = qN_{ss1}$, and $C_{ss2} = qN_{ss2}$. N_{ss1} and N_{ss2} are the interface state density at the front and back of the SOI, respectively. Applying these two correction factors, we now have

$$S \equiv \frac{\partial V_g}{\partial(\log(I_d))} = \frac{1}{\lambda} C \frac{kT}{q} \ln 10. \tag{A6}$$

Equations (A6), (A5), and (A4) can be used to calculate S as a function of L using only the thickness and permittivity of the materials stack, as well as the front and back interface state density. For the devices fabricated in this work, $t_{box} = 145$ nm, $t_{Si} = 35$ nm, and the measured t_{ox} values of 3.71 nm and 3.33 nm are used for PE-ALD and sputtered devices, respectively. The back interface state density is neglected, and the front interface state density N_{ss1} is calculated to be 3×10^{11} cm^{-2} from a best fit of Eq. (A6) to the measured data. The model and data are graphed in Fig. 10, which show that the increase in S with decreasing gate length and the small increase in S for the ALD devices with thicker t_{ox} compared to PVD devices is well matched to what is predicted by the model.

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